In the Claims:

Claim 1 (currently amended): An interposer for compliantly connecting a chip die directly to a circuit card comprising a layer of elastic dielectric material having an array of metal plated vias extending from one surface of said dielectric material to the other with each of said metal plated vias terminating in a metal pad at said one and said other surface and with each of said metal plated vias similarly sloped with respect to said one and said other surface so as to allow said interposer to flex both vertically and horizontally.

Claim 2 (original) The interposer as set forth in Claim 1 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

Claim 3 (original) The interposer as set forth in Claim 2 wherein said elastic dielectric material has an array of holes therethrough positioned between said array of copper plated vias.

Claim 4 (original) The interposer as set forth in Claim 3 wherein said elastic dielectric material is 10 to 15 mils thick and has an elastic modulus in the range of 50,000 to 400,000 psi.

5. (currently amended) An electronic package comprising:

a semiconductor chip die having an array of conductive pads on one surface thereof;

a flexible layer of dielectric material having an array of metal plated vias extending therethrough in similarly sloped relationship to opposing surfaces thereof so as to allow said layer of dielectric material to flex both vertically and horizontally ~~with said array of metal plated vias on one surface corresponding to said array of conductive pads on said chip die~~ and with each of said vias terminating in a metal pad on each of said opposing surfaces to form an array of pads thereon with respective ones of ~~with each~~ said metal ~~pad~~ pads on ~~said~~ one of said opposing surfaces ~~surface~~ electrically connected to respective ones of said array of conductive pads on said chip die; and

a circuit card having an array of conductive pads corresponding to said array of metal pads on the other of said opposing surfaces of said flexible layer of dielectric material with respective ones of said array of conductive pads on said circuit card electrically connected to respective ones of said array of metal pads on the said other of said opposing surfaces of said layer of dielectric material ~~and connected by solder thereto~~.

Claim 6. (original) The electronic package of Claim 5 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

Claim 7 (currently amended) The electronic package of Claim 5 wherein each of said metal plated vias of said array of metal plated vias is formed by two segments each of which is sloped with respect to an opposing surface of said flexible layer of dielectric material and meet internal to said surfaces to form a V-shaped metal plated via.

Claim 8 (previously canceled)

Claim 9 (currently amended) The electronic package of Claim 6 wherein said flexible layer of dielectric material has an array of holes therethrough positioned between said array of copper plated vias.

Claim 10 (currently amended) The electronic package of Claim 6 wherein respective ones of ~~each of~~ said copper pads on said one of said surfaces are ~~respectively~~ connected to respective ones of said array of conductive pads on said chip die by a copper plated connection.

Claim 11 (original) The electronic package of Claim 5 wherein said flexible layer is a low elastic modulus material.

Claim 12 (original) The electronic package of Claim 5 wherein said flexible layer has an elastic modulus in the range of 50,000 to 400,000 psi.

Claim 13 (previously amended) The electronic package of Claim 6 wherein said copper plated vias are filled with solder.

Claims 14 - 22 (withdrawn).